UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,861	10/29/2003	Hiroshi Makamura	244682US2S	5717

22850 7590 07/25/2005

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
NGUYEN, NAM THANH	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,861	MAKAMURA ET AL.	
	Examiner	Art Unit	
	Nam T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,12 and 13* is/are rejected.

7)☒ Claim(s) *9-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/29/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *EAST SEARCH*.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 1-8 and 12-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Hosono et al. (Pub. No.: US 2003/0214853).

For the purpose of this rejection, a first pass/fail signal is considered as a program verify signal of a program verify control function.

Regarding claim 1, Hosono et al. disclose a plurality of memory cell arrays (pages, see paragraph 0122) constituted of a plurality of memory cells or memory cell units (B1, see fig. 2) which consists of a plurality of memory cells, arranged in a matrix, (it is clearly stated in fig. 2 and paragraph [0045]) wherein the plurality of memory cell arrays constitute a plurality of cell array groups each of which consists of two or more memory cell arrays, (see paragraph [0046]) and a first Pass/Fail signal (the verify signal of erratic program verify) indicative of success or failure of an operation is outputted in accordance with each cell array group (see paragraph [0044 and 0057]).

Regarding claim 2, a parallel operation with respect to memory cells in two or more of the plurality of cell array groups. It is clearly explained in the paragraph [0046].

Regarding claim 3, paragraph [0009] of Hosono et al. disclose a parallel operation with respect to memory cells in two or more of the plurality of cell arrays.

Regarding claim 4, the operation is a program operation (see paragraph [0017]).

Regarding claim 5, the first Pass/Fail signal is a Pass/Fail signal (program verify signal is performed by 403 of fig. 1) indicating whether the operation has attained success with respect to all of selected memory cells (as stated in paragraph 0009) included in each of the cell array groups (page) or not.

Regarding claim 6, a second Pass/Fail signal (a flag signal that is generated by 402 of fig. 1) of an entire chip (EEPROM chip) is also outputted when the first Pass/Fail signal is outputted (see paragraphs 0088 and 0098).

Regarding claim 7, a Pass/Fail signal (the verify signal) indicating whether the operation has attained success with respect to one memory cell array (100 of fig. 1) selected from the two or more memory cell arrays in each of the cell array groups or not (see paragraph 0010).

Regarding claim 8, the first Pass/Fail signal is outputted after a first command is inputted (see paragraph 0098).

Regarding claim 12 and 13, the paragraph 005 of Hosono et al. disclose the memory is EEPROM and the memory cell unit is a NAND cell type.

Allowable Subject Matter

3. Claims 9-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the prior art to:

"a third Pass/Fail signal which is different from the first Pass/Fail signal is outputted after a second command is inputted" as claimed in the dependent claim 9; or

"a forth Pass/Fail signal is outputted with respect to each of the cell arrays included in an entire chip after a third command is input" as claimed in the dependent claim 10.

Conclusion

4. The following prior art, which is considered pertinent to applicant's disclosure although not relied upon, includes:

Sakui et al. US. Pat no. 6,031,760) or Chen et ál. Pub. No.: US 2004/0145952) disclose EEPROM cell array with pass/fail function similar to that of the present application, but fail to disclose the claimed limitations as described above.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nam T. Nguyen whose telephone number is (571) 272-1878. The examiner can normally be reached on 8 am to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nam T Nguyen
Examiner
Art Unit 2824

7/11/05
***

7/12/05

RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800